

CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters PATENT is:

- 1 1. A silicon-on-insulator (SOI) metal oxide field effect transistor (MOSFET) device
2 comprising:
3
4 an implanted back-gate region located atop an oxide layer, wherein a surface portion of
5 said implanted back-gate region includes a back-gate oxide formed thereon;
6
7 a body region located atop said back-gate oxide;
8
9 a gate dielectric located atop a surface portion of said body region; and
10
11 a polysilicon gate located atop a portion of said gate dielectric.
12
- 1 2. The SOI MOSFET of Claim 1 further comprising back-gate-STI regions located
2 under portions of said body region.
- 1 3. The SOI MOSFET device of Claim 1 wherein said body region further includes
2 source/drain regions and source/drain extension regions.
- 1 4. The SOI MOSFET device of Claim 1 wherein said polysilicon gate includes spacers
2 on sidewalls thereof.
- 1 5. The SOI MOSFET device of Claim 1 further comprising raised source/drain regions
2 located atop a portion of said body region.

1 6. The SOI MOSFET device of Claim 1 further comprising silicide regions located
2 atop a portion of said body region and atop the polysilicon gate.

1 7. The SOI MOSFET device of Claim 1 further comprising a dielectric material
2 encapsulating said polysilicon gate.

1 8. The SOI MOSFET device of Claim 7 wherein said dielectric material includes
2 conductive filled contact holes.

1 9. The SOI MOSFET device of Claim 1 wherein said implanted back-gate serves as a
2 threshold control system for the polysilicon gate.

1 10. A method of fabricating a silicon-on-insulator (SOI) metal oxide field effect
2 transistor (MOSFET) device comprising the steps of:

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4 providing a structure including at least a back-gate oxide located atop a Si-containing
5 layer, said Si-containing layer is a component of a SOI wafer;

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7 forming alternating regions of back-gate-STI and first polysilicon atop said back-gate
8 oxide;

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10 forming a second polysilicon layer atop said alternating regions of back-gate-STI and
11 first polysilicon;

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13 implanting a back-gate region into said polysilicon layers;

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15 forming an oxide layer on said second polysilicon layer;

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17 bonding a holding-substrate wafer to said oxide layer and flipping the bonded structure
18 to expose layers of said SOI wafer;

19 removing selective layers of said SOI wafer stopping on said Si-containing layer;
20
21 converting a portion of said Si-containing layer into a body region; and
22
23 forming a gate dielectric and a polysilicon gate atop said body region.

1 11. The method of Claim 10 further comprising forming raised source/drain regions
2 atop said body region that lays adjacent to said polysilicon gate.

1 12. The method of Claim 11 further comprising converting said raised source/drain
2 regions into silicide regions.

1 13. The method of Claim 10 wherein said bonding is performed at a temperature of
2 about 900°C to about 1100°C for a time period of from about 1.5 hours to about 2.5
3 hours.

1 14. The method of Claim 10 wherein said bonding is performed at a temperature of
2 from about 18°C to about 27°C in an inert ambient.

1 15. The method of Claim 10 wherein said body region is formed by a masked ion
2 implantation process.

1 16. The method of Claim 10 wherein said alternating polysilicon region have under-cut
2 sidewalls.

1 17. The method of Claim 10 further comprising encapsulating said polysilicon gate
2 with a dielectric material, said dielectric material having conductively filled contact
3 holes abutting said polysilicon gate.